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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/021,497	12/19/2001	William G. En	50432-477	1401

7590 10/21/2003

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EXAMINER	
SOWARD, IDA M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 10/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/021,497	EN ET AL.	
	Examiner	Art Unit	
	Ida M Soward	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8 and 10-23* is/are pending in the application.

4a) Of the above claim(s) *11-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8,10 and 21-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action is in response to the Applicants' amendment filed July 25, 2003.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, 8, 10 and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art Figure 7 in view of Tuan et al. (US 2002/0151141 A1) and Baliga (US 2002/0177277 A1).

Admitted Prior Art Figure 7 teaches a wafer comprising: a base layer **42**; an active region in the base; a gate dielectric layer **46** formed on the active region; a conductive layer **50** formed on the gate dielectric layer; a plurality of shallow trench isolation regions **44** formed in the wafer; and a metal interconnect layer **54** formed over the conductive layer. However, Admitted Prior Art Figure 7 fails to teach a wafer being divided into a plurality of first, second and third portions. Tuan et al. teach a wafer being divided into a plurality of first, second and third portions; the first portion comprise gate dielectric capacitor (a transistor), the gate dielectric capacitors comprise a first electrode layer **124**, an insulating layer **108**, and a second electrode layer **128** made of polysilicon

contacting an isolation region **1010;** wherein the first electrode layer is formed from the active layer, the insulating layer is formed from the gate dielectric layer, and the second electrode is formed from the conductive layer; and the third portions (containing no active layer) comprise second dummy structures **141**, the second dummy structures comprise an insulating layer and a second electrode layer; wherein the insulating layer of the second dummy structures is formed from an isolation region **1010** and the second electrode layer of the second dummy structures if formed from the conductive layer (Figure 3, page 3, paragraphs [0034]-[0042]). Baliga teaches the second portions comprise first dummy structures **118c**, the first dummy structures comprise a first electrode layer and an insulating layer; wherein the first electrode layer of the first dummy structures is formed from the doped silicon active layer **32** and the insulating layer of the first dummy structures is formed from the gate dielectric layer and not containing a conductive layer (Figure 11, page 8, paragraph [0056]). Since Admitted Prior Art Figure 7, Tuan et al. and Baliga are from the same field of endeavor (semiconductor devices), the purposed disclosed by Baliga would have been recognized in the pertinent art of Admitted Prior Art Figure 7 and Tuan et al. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the gate dielectric structure of Admitted Prior Art Figure 7 with the first, second and third portions of Tuan et al. and the dummy structures of Baliga to provide a structure that can support high voltages (page 2, paragraph [0013]).

Response to Arguments

Applicant's arguments filed 07-25-03 have been fully considered but they are not persuasive.

In response to the remarks on page 8, first paragraph, Figure 3 of Tuan et al. disclose dummy structures 141 and multiple portions 901, 4402, 4404 and 4406. Further, the combination of Tuan et al. and Baliga disclose the claimed first electrode layer, as required by claim 21 in that Tuan et al. disclose the first portion comprise gate dielectric capacitor (a transistor), the gate dielectric capacitors comprise a first electrode layer **124**, an insulating layer **108**, and a second electrode layer **128**, wherein the first electrode layer is formed from the active layer, the insulating layer is formed from the gate dielectric layer, and the second electrode is formed from the conductive layer; and Baliga discloses an active layer comprising source/drain regions. In response to the remarks on page 8, second paragraph, 124 and 128 of Tuan et al. are separate and distinct electrode layers. In response to the remarks on page 8, fifth paragraph, claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function. In re Danly, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). In regard to the remarks on page 9, first paragraph, since Tuan et al. and Baliga are from the same field of endeavor (semiconductor devices having dummy structures), the purposed disclosed by Baliga would have been recognized in the pertinent art of Tuan et al. In response to the remarks on pages 9-10, second-third and first paragraphs, respectively, In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can

only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the motivation to so can be found in Tuan et al. (page 2, paragraph [0013]).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M Soward whose telephone number is 703-305-

3308. The examiner can normally be reached on Monday - Thursday, 6:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ims
October 16, 2003

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800